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EXAMINER	
SAVLA, ARPAN P	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	10/724,164	HIROSE, YUKITOSHI	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the corresp ndence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/1/03, 6/6/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10/724,164 has a total of 38 claims pending in the application, there are 6 independent claims and 32 dependent claims, all of which are ready for examination by the Examiner.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

1. Applicant's oath/declaration has been reviewed by the Examiner and is found to conform to the requirements prescribed in 37 CFR 1.63.

STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

2. As required by MPEP § 201.14(c), acknowledgment is made of Applicant's claim for priority based on an application filed in the Japanese Patent Office on December 2, 2002.

INFORMATION CONCERNING DRAWINGS

Drawings

3. Applicant's drawings submitted April 9, 2004 are acceptable for examination.

ACKNOWLEDGMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

4. As required by MPEP § 609(c), Applicant's submission of the Information Disclosure Statements dated December 1, 2003 and June 6, 2005 are acknowledged by the Examiner and the some of the cited references have been considered in the examination of the claims now pending. As required by MPEP § 609 c(2), a copy of the PTOL-1449 initialed and dated by the Examiner is attached to the instant office action.

5. The Information Disclosure Statement (IDS) filed June 6, 2005 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 (see reasons directly below). It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this IDS or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

6. All three references on the Information Disclosure Statement dated June 6, 2005 have **not** been considered by the Examiner because the references do not comply with 37 CFR 1.98 (a)(3)(ii). The references are non-English-language documents, however, there is no copy of an English-language translation of the documents, or portion thereof.

OBJECTIONS

Specification

7. The disclosure is objected to because it contains an embedded hyperlink and/or other form of browser-executable code on page 2, line 20. Applicant is required to delete the embedded hyperlink and/or other form of browser-executable code. See MPEP § 608.01.

8. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Hot Swapping Of Memory Modules Configured In A Ring Bus."

Appropriate correction is required.

Claims

9. **Claims 15-16 and 33-34** are objected to because of the following informalities: In line 2 of each claim respectively, the phrase "memory for mirror" is vague and indefinite. Applicant may consider amending the claims to read "memory for mirroring."

Appropriate correction is required.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 1-2 and 21-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. **Claims 1-2 and 21-22** recite the limitation "switching said bus" in lines 7, 9, 9, and 9 respectively. There is insufficient antecedent basis for this limitation in the claims. Applicant may consider amending the claims to read "switching a bus."

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 1 and 21 are rejected under 35 U.S.C. 103(a) as being obvious over Applicant's "Description of the Prior Art" appearing in Applicant's specification, hereafter referred to as "Applicant's admitted prior art" in view of Chow et al. (U.S. Patent Application Publication 2002/0069317).

15. **As per claim 1**, Applicant's admitted prior art discloses a memory system comprising:

a plurality of memory modules provided with memory areas for holding data and buffer sections for sending and receiving the data (pg. 2, lines 14-17; Fig. 2), elements 112_{1-4});

a control device for, in replacing an arbitrary memory module, switching said bus from a unidirectional bus capable of sending and receiving a signal unidirectionally to a bi-directional bus capable of sending and receiving a signal bi-directionally (pg. 2, line 25 – pg. 3, line 5; Fig. 2, element 113); *It should be noted that "memory controller" is analogous to "control device." It should be noted as disclosed in the specification the two unidirectional buses provide unidirectional functionality when used separately as well as bi-directional functionality when used together.*

a CPU which controls said control device for access operation to said memory modules (Fig. 2, element 111),

wherein said buffer sections are connected in series to form a ring bus with said control device, each having a buffer circuit for causing said bus to operate as said unidirectional bus or said bi-directional bus in accordance with an instruction from said control device (pg. 2, lines 14-17; pg. 2, line 21 – pg. 3, line 5; Fig. 2).

Applicant's admitted prior art admitted prior art does not expressly disclose a hard disk device to which the data stored in said memory modules is copied;

a control device for detecting an address space of said memory module to be replaced, and accessing a memory area in said hard disk device corresponding to the detected address space at the time when an access to said memory module to be replaced is requested.

Chow discloses a hard disk device to which the data stored in said memory modules is copied (paragraph 135; Fig. 14, elements 110, 130, and 425); *It should*

noted that "non-volatile storage module" is analogous to "hard disk device" and "memory matrix module" is analogous to "memory module."

a control device for detecting an address space of said memory module to be replaced, and accessing a memory area in said hard disk device corresponding to the detected address space at the time when an access to said memory module to be replaced is requested (paragraph 0168; Fig. 14, element 125). *It should be noted that "management module" is analogous to "control device." It should also be noted that in order for the failover process to be completely transparent to the data processing system it is inherently required the management module detect a memory space in the failed memory matrix module and subsequently access a memory area in the non-volatile storage module corresponding to the detected address space when an access to the memory matrix module that failed is requested.*

Applicant's admitted prior art and Chow are analogous art because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Chow's non-volatile storage module and management module within Applicant's admitted prior art's RAMLINK memory system.

The motivation for doing so would have been to minimize delay when the memory matrix failed by providing failover to a backup memory that is completely transparent to a user of the data processing system (Chow, paragraph 0168).

Therefore, it would have been obvious to combine Applicant's admitted prior art and Chow for the benefit of obtaining the invention as specified in claim 1.

16. **As per claim 21**, Applicant's admitted prior art discloses a control method for a memory system which has a plurality of memory modules provided with memory areas for holding data and buffer sections for sending and receiving the data (pg. 2, lines 14-17; Fig. 2, elements 112_{1-4}),

wherein said buffer sections are connected in series to form a ring bus with a control device which controls an operation for accessing memory modules (pg. 2, lines 14-17; Fig. 2), said method comprising the steps of:

in replacing an arbitrary memory module, switching said bus from a unidirectional bus capable of sending and receiving a signal unidirectionally to a bi-directional bus capable of sending and receiving a signal bi-directionally (pg. 2, line 25 – pg. 3, line 5; Fig. 2, element 113). *It should be noted as disclosed in the specification the two unidirectional buses provide unidirectional functionality when used separately as well as bi-directional functionality when used together.*

Chow discloses copying the data stored in said memory modules to a hard disk device at each predetermined period paragraph 135; Fig. 14, elements 110, 130, and 425); *It should noted that "non-volatile storage module" is analogous to "hard disk device" and "memory matrix module" is analogous to "memory module."*

detecting an address space of said memory module to be replaced (paragraph 0168; Fig. 14, element 125);

and accessing a memory area in said hard disk device corresponding to the detected address space at the time when an access to said memory module to be replaced is requested (paragraph 0168; Fig. 14, element 125). *It should be noted that*

in order for the failover process to be completely transparent to the data processing system it is inherently required the management module detect a memory space in the failed memory matrix module and subsequently access a memory area in the non-volatile storage module corresponding to the detected address space when an access to the memory matrix module that failed is requested.

Please see the 103 rejection of claim 1 above for the reasons to combine Applicant's admitted prior art and Chow.

17. Claims 2, 15, 17, 19, 22, 33, 35, and 37 are rejected under 35 U.S.C. 103(a) as being obvious over Applicant's admitted prior art in view of Lasker et al. (U.S. Patent 5,586,291).

18. **As per claim 2**, Applicant's admitted prior art discloses a memory system comprising:

a plurality of memory modules provided with memory areas for holding data and buffer sections for sending and receiving the data (pg. 2, lines 14-17; Fig. 2, elements 112_{1-4});

a control device for, in replacing an arbitrary memory module, switching said bus from a unidirectional bus capable of sending and receiving a signal unidirectionally to a bi-directional bus capable of sending and receiving a signal bi-directionally (pg. 2, line 25 – pg. 3, line 5; Fig. 2, element 113); *Please see the citation note for the similar limitation in claim 1 above.*

a CPU which controls said control device for access operation to said memory modules (Fig. 2, element 111),

wherein said buffer sections are connected in series to form a ring bus with said control device, each having a buffer circuit for causing said bus to operate as said unidirectional bus or said bi-directional bus in accordance with an instruction from said control device (pg. 2, lines 14-17; pg. 2, line 21 – pg. 3, line 5; Fig. 2).

Applicant's admitted prior art admitted prior art does not expressly disclose a hard disk device to which the data stored in said memory modules is copied;

a storage to which data stored in an arbitrary memory module is temporarily copied

a control device for detecting an address space of said memory module to be replaced, copying data corresponding to the detected address space from said hard disk device to said storage, and accessing a memory area in said storage corresponding to the detected address space at the time when an access to said memory module to be replaced is requested.

Lasker discloses a hard disk device to which the data stored in said memory modules is copied (col. 7, line 26; Fig. 1, element 18); *It should noted that "disk drive" is analogous to "hard disk device."*

a storage to which data stored in an arbitrary memory module is temporarily copied (col. 9, lines 42-43; Fig. 2, elements 34a' and 34b'); *It should noted that "NVSIMM 34b'" is analogous to "memory module" and "NVSIMM 34a' " is analogous to "storage."*

a control device for detecting an address space of said memory module to be replaced, copying data corresponding to the detected address space from said hard

disk device to said storage, and accessing a memory area in said storage corresponding to the detected address space at the time when an access to said memory module to be replaced is requested (col. 9, lines 38-48; Fig. 2, elements 40, 34a', and 34b'). *It should be noted that "cache memory control circuit" is analogous to "control device." It should be also be noted that when NVSIMM 34a' is placed into a different controller for the failed NVSIMM 34b' it is inherently required cache memory control circuit detect an address space of NVSIMM 34b', copy data corresponding to the detected address space (i.e. the same data corresponding to the detected address space from said hard disk device) from NVSIMM 34b' to NVSIMM 34a', and then access a memory area in NVSIMM 34a' at the time when an access to NVSIMM 34b' is requested.*

Applicant's admitted prior art and Lasker are analogous art because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Lasker's mirror mode modules within Applicant's admitted prior art's RAMLINK memory system.

The motivation for doing so would have been to reduce the potential for data loss (Lasker, col. 9, line 49).

Therefore, it would have been obvious to combine Applicant's admitted prior art and Chow for the benefit of obtaining the invention as specified in claim 2.

19. **As per claim 15**, the combination of Applicant's admitted prior art/Lasker discloses said storage is a memory module for mirror which is provided with a memory

area for holding data and a buffer section for sending and receiving data (Lasker, col. 9, lines 38-43; Fig. 2, element 34a'). *It should be noted that in order for any data to be written to and copied from the NVSIMM 34a' it is inherently required the NVSIMM 34a' have a some sort of "buffer section."*

20. **As per claim 17**, the combination of Applicant's admitted prior art/Lasker discloses said storage is a memory for graphics (Lasker, col. 9, lines 38-43; Fig. 2, element 34a'). *It should be noted that this limitation is merely an intended use of the claimed invention. Since Lasker's NVSIMM 34a' is capable of performing the intended use (i.e. capable of being a graphics memory), it therefore meets the claim.*

21. **As per claim 19**, the combination of Applicant's admitted prior art/Lasker discloses said storage is free memory areas of the other memory modules excluding said memory module to be replaced (Lasker, col. 9, lines 38-43; Fig. 2, element 34a'). *It should be noted that NVSIMM 34b' is the failed memory module to be replaced and the mirrored data is stored on the free area of NVSIMM 34a' (i.e. another memory module which is not the memory module being replaced).*

22. **As per claim 22**, Applicant's admitted prior art discloses a control method for a memory system which has a plurality of memory modules provided with memory areas for holding data and buffer sections for sending and receiving the data (pg. 2, lines 14-17; Fig. 2, elements 112_{1-4}),

wherein said buffer sections are connected in series to form a ring bus with a control device which controls an operation for accessing memory modules (pg. 2, lines 14-17; Fig. 2), said method comprising the steps of:

in replacing an arbitrary memory module, switching said bus from a unidirectional bus capable of sending and receiving a signal unidirectionally to a bi-directional bus capable of sending and receiving a signal bi-directionally (pg. 2, line 25 – pg. 3, line 5; Fig. 2, element 113); *Please see the citation note for the similar limitation in claim 2 above.*

Lasker discloses copying the data stored in said memory modules to a hard disk device at each predetermined period (col. 7, line 26; Fig. 1, element 18); *It should noted that "disk drive" is analogous to "hard disk device."*

detecting an address space of said memory module to be replaced; copying data corresponding to the detected address space from said hard disk device to a storage (col. 9, lines 38-48; Fig. 2, elements 40, 34a', and 34b');

and accessing a memory area in said storage corresponding to the detected address space at the time when an access to said memory module to be replaced is requested (col. 9, lines 38-48; Fig. 2, elements 40, 34a', and 34b'). *It should be noted that "cache memory control circuit" is analogous to "control device." It should be also be noted that when NVSIMM 34a' is placed into a different controller for the failed NVSIMM 34b' it is inherently required cache memory control circuit detect an address space of NVSIMM 34b', copy data corresponding to the detected address space (i.e. the same data corresponding to the detected address space from said hard disk device) from NVSIMM 34b' to NVSIMM 34a', and then access a memory area in NVSIMM 34a' at the time when an access to NVSIMM 34b' is requested.*

Please see the 103 rejection of claim 2 above for the reasons to combine Applicant's admitted prior art and Lasker.

23. **As per claim 33**, the combination of Applicant's admitted prior art/Lasker discloses said storage is a memory for mirror provided with a memory area for holding data and a buffer section for sending and receiving data (Lasker, col. 9, lines 38-43; Fig. 2, element 34a'). *Please see the citation note for claim 15 above.*

24. **As per claim 35**, the combination of Applicant's admitted prior art/Lasker discloses said storage is a memory for graphics (Lasker, col. 9, lines 38-43; Fig. 2, element 34a'). *Please see the citation note for claim 17 above.*

25. **As per claim 37**, the combination of Applicant's admitted prior art/Lasker discloses said storage is free memory areas of the other memory modules excluding said memory module to be replaced (Lasker, col. 9, lines 38-43; Fig. 2, element 34a'). *Please see the citation note for claim 19 above.*

26. Claims 5, 8, 16, 18, 20, 23, 26, 34, 36, and 38 are rejected under 35 U.S.C. 103(a) as being obvious over Applicant's admitted prior art in view of Lasker and Funaba et al. (U.S. Patent 6,411,539).

27. **As per claim 5**, the combination of Applicant's admitted prior art/Lasker discloses a memory system comprising:

a plurality of memory modules provided with memory areas for holding data and buffer sections for sending and receiving the data (Applicant's admitted prior art, pg. 2, lines 14-17; Fig. 2, elements 112_{1-4});

a hard disk device to which the data stored in said memory modules is copied (Lasker, col. 7, line 26; Fig. 1, element 18); *Please see the citation note for the similar limitation in claim 2 above.*

a storage to which data stored in an arbitrary memory module is temporarily copied (Lasker, col. 9, lines 42-43; Fig. 2, elements 34a' and 34b'); *Please the citation note for the similar limitation in claim 2 above.*

a control device for, in replacing an arbitrary memory module, detecting an address space of said memory module to be replaced, copying data corresponding to the detected address space from said hard disk device to said storage, and accessing a memory area in said storage corresponding to the detected address space at the time when an access to said memory module to be replaced is requested (Lasker, col. 9, lines 38-48; Fig. 2, elements 40, 34a', and 34b'); *Please the citation note for the similar limitation in claim 2 above.*

and a CPU which controls said control device for access operation to said memory modules (Applicant's admitted prior art, Fig. 2, element 111),

wherein said buffer sections are connected in series to form a unidirectional bus capable of sending and receiving a signal unidirectionally (pg. 2, lines 25 – pg. 3, line 2; Fig. 2).

Please see the 103 rejection of claim 2 above for the reasons to combine Applicant's admitted prior art and Lasker.

The combination of Applicant's admitted prior art/Lasker does not expressly disclose a short-circuit device for, in replacing an arbitrary memory module, recovering bus connection which is disconnected by removing said memory module to be replaced.

Funaba discloses a short-circuit device for, in replacing an arbitrary memory module, recovering bus connection which is disconnected by removing said memory module to be replaced (col. 21, lines 8-31; Fig. 34; Fig. 35). *It should be noted that "dummy module" is analogous to "short-circuit device."*

The combination of Applicant's admitted prior art/Lasker and Funaba are analogous because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Funaba's dummy module within Applicant's admitted prior art/Lasker's memory module system.

The motivation for doing so would have been to change the memory capacity of the memory system without producing branching in the paths of the signal wirings, thus causing an increase in wiring length (Funaba, col. 21, lines 28-31).

Therefore, it would have been obvious to combine Applicant's admitted prior art, Lasker, and Funaba for the benefit of obtaining the invention as specified in claim 5.

28. **As per claim 8**, the combination of Applicant's admitted prior art/Lasker discloses said short-circuit device is a dummy module which is inserted instead of said memory module to be replaced and is provided with a short-circuit line for short-

circuiting bus connection which is disconnected by removing said memory module (Funaba, col. 21, lines 8-31; Fig. 34; Fig. 35).

29. **As per claim 16**, the combination of Applicant's admitted prior art/Lasker discloses said storage is a memory module for mirror which is provided with a memory area for holding data and a buffer section for sending and receiving data (Lasker, col. 9, lines 38-43; Fig. 2, element 34a'). *Please see the citation note for claim 15 above.*

30. **As per claim 18**, the combination of Applicant's admitted prior art/Lasker discloses said storage is a memory for graphics (Lasker, col. 9, lines 38-43; Fig. 2, element 34a'). *Please see the citation note for claim 17 above.*

31. **As per claim 20**, the combination of Applicant's admitted prior art/Lasker discloses said storage is free memory areas of the other memory modules excluding said memory module to be replaced (Lasker, col. 9, lines 38-43; Fig. 2, element 34a'). *Please see the citation note for claim 19 above.*

32. **As per claim 23**, the combination of Applicant's admitted prior art/Lasker discloses a control method for a memory system which has a plurality of memory modules provided with memory areas for holding data and buffer sections for sending and receiving the data (Applicant's admitted prior art, pg. 2, lines 14-17; Fig. 2, elements 112_{1-4}),

wherein said buffer sections are connected in series to form a unidirectional bus capable of sending and receiving a signal unidirectionally (Applicant's admitted prior art, pg. 2, line 25 – pg. 3, line 2; Fig. 2), said method comprising the steps of:

copying the data stored in said memory modules to a hard disk device at each predetermined period (Lasker, col. 7, line 26; Fig. 1, element 18); *Please see the citation note for the similar limitation in claim 22 above.*

detecting an address space of said memory module to be replaced; copying data corresponding to the detected address space from said hard disk device to a storage (Lasker, col. 9, lines 38-48; Fig. 2, elements 40, 34a', and 34b'); *Please see the citation note for the similar limitation in claim 22 above.*

and accessing a memory area in said storage corresponding to the detected address space at the time when an access to said memory module to be replaced is requested (Lasker, col. 9, lines 38-48; Fig. 2, elements 40, 34a', and 34b'); *Please see the citation note for the similar limitation in claim 22 above.*

The combination of Applicant's admitted prior art/Lasker does not expressly disclose replacing an arbitrary memory module, short-circuiting bus connection which is disconnected by removing said memory module to be replaced.

Funaba discloses replacing an arbitrary memory module, short-circuiting bus connection which is disconnected by removing said memory module to be replaced (col. 21, lines 8-31; Fig. 34; Fig. 35).

Please see the 103 rejection of claim 5 above for the reasons to combine Applicant's admitted prior art, Lasker, and Funaba.

33. **As per claim 26**, the combination of Applicant's admitted prior art/Lasker discloses in replacing an arbitrary memory module, inserting a dummy module provided with a short-circuit line for short-circuiting a bus, which is disconnected by removing said

memory module, instead of said memory module to be replaced (Funaba, col. 21, lines 8-31; Fig. 34; Fig. 35).

34. **As per claim 34**, the combination of Applicant's admitted prior art/Lasker discloses said storage is a memory for mirror provided with a memory area for holding data and a buffer section for sending and receiving data (Lasker, col. 9, lines 38-43; Fig. 2, element 34a'). *Please see the citation note for claim 15 above.*

35. **As per claim 36**, the combination of Applicant's admitted prior art/Lasker discloses said storage is a memory for graphics (Lasker, col. 9, lines 38-43; Fig. 2, element 34a'). *Please see the citation note for claim 17 above.*

36. **As per claim 38**, the combination of Applicant's admitted prior art/Lasker discloses said storage is free memory areas of the other memory modules excluding said memory module to be replaced (Lasker, col. 9, lines 38-43; Fig. 2, element 34a'). *Please see the citation note for claim 19 above.*

37. Claims 3, 6, and 24 are rejected under 35 U.S.C. 103(a) as being obvious over Applicant's admitted prior art in view of Chow as applied to claims 1 and 21 above, and in further view of Funaba.

38. **As per claim 3**, the combination of Applicant's admitted prior art/Chow discloses all the limitations of claim 3 except a short-circuit device for, when an arbitrary memory module is replaced, recovering bus connection which is disconnected by removing said memory module.

Funaba discloses a short-circuit device for, when an arbitrary memory module is replaced, recovering bus connection which is disconnected by removing said memory

module (col. 21, lines 8-31; Fig. 34; Fig. 35). *It should be noted that "dummy module" is analogous to "short-circuit device."*

The combination of Applicant's admitted prior art/Chow and Funaba are analogous because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Funaba's dummy module within Applicant's admitted prior art/Chow's memory module system.

The motivation for doing so would have been to change the memory capacity of the memory system without producing branching in the paths of the signal wirings, thus causing an increase in wiring length (col. 21, lines 8-31; Fig. 34; Fig. 35).

Therefore, it would have been obvious to combine Applicant's admitted prior art, Chow, and Funaba for the benefit of obtaining the invention as specified in claim 3.

39. **As per claim 6**, the combination of Applicant's admitted prior art/Lasker/Funaba discloses said short-circuit device is a dummy module which is inserted instead of said memory module to be replaced and is provided with a short-circuit line for short-circuiting bus connection which is disconnected by removing said memory module (Funaba, col. 21, lines 8-31; Fig. 34; Fig. 35).

40. **As per claim 24**, the combination of Applicant's admitted prior art/Lasker/Funaba discloses replacing an arbitrary memory module, inserting a dummy module provided with a short-circuit line for short-circuiting a bus, which is disconnected by removing said

memory module, instead of said memory module to be replaced (Funaba, col. 21, lines 8-31; Fig. 34; Fig. 35).

41. **Claims 4, 7, and 25 are rejected under 35 U.S.C. 103(a) as being obvious over Applicant's admitted prior art in view of Lasker as applied to claims 2 and 22 above, and in further view of Funaba.**

42. **As per claim 4**, the combination of Applicant's admitted prior art/Lasker disclose all the limitations of claim 4 except a short-circuit device for, when an arbitrary memory module is replaced, recovering bus connection which is disconnected by removing said memory module.

Funaba discloses a short-circuit device for, when an arbitrary memory module is replaced, recovering bus connection which is disconnected by removing said memory module (col. 21, lines 8-31; Fig. 34; Fig. 35). *It should be noted that "dummy module" is analogous to "short-circuit device."*

Please see the 103 rejection of claim 5 above for the reasons to combine Applicant's admitted prior art, Lasker, and Funaba.

43. **As per claim 7**, the combination of Applicant's admitted prior art/Lasker/Funaba discloses said short-circuit device is a dummy module which is inserted instead of said memory module to be replaced and is provided with a short-circuit line for short-circuiting bus connection which is disconnected by removing said memory module (Funaba, col. 21, lines 8-31; Fig. 34; Fig. 35).

44. **As per claim 25**, the combination of Applicant's admitted prior art/Lasker/Funaba discloses replacing an arbitrary memory module, inserting a dummy module provided

with a short-circuit line for short-circuiting a bus, which is disconnected by removing said memory module, instead of said memory module to be replaced (Funaba, col. 21, lines 8-31; Fig. 34; Fig. 35).

45. Claims 9 and 27 are rejected under 35 U.S.C. 103(a) as being obvious over Applicant's admitted prior art in view of Chow and Funaba as applied to claims 3 and 21 above, and in further view of Emerson et al. (U.S. Patent 6,487,623).

46. **As per claim 9**, the combination of the combination of Applicant's admitted prior art/Chow/Funaba discloses all the limitations of claim 9 except said short-circuit device is an FET switch, which is provided in association with said memory modules, respectively, for short-circuiting or opening bus connection which is disconnected by removing said memory module,

and in replacing an arbitrary memory module, said control device generates a control signal for turning ON the FET switch provided in association with said memory module to be replaced and turning OFF the FET switches provided in association with the other memory modules.

Emerson discloses said short-circuit device is an FET switch, which is provided in association with said memory modules, respectively, for short-circuiting or opening bus connection which is disconnected by removing said memory module (col. 7, lines 12-25; Fig. 4, element 160), *It should be noted "FET signal isolation buffer" is analogous to "FET switch."*

and in replacing an arbitrary memory module, said control device generates a control signal for turning ON the FET switch provided in association with said memory

module to be replaced and turning OFF the FET switches provided in association with the other memory modules (col. 10, lines 37-45; col. 9, lines 38-41; Fig. 4, elements 160 and 164). *It should be noted that "hot-plug controller" is analogous to "control device." It should be noted that the FET isolation buffer's "disconnect" mode is analogous to the "turning ON the FET switch" and conversely the FET isolation buffer's "connect" mode is analogous to "turning OFF the FET switch." The actual states of "ON" and "OFF" are arbitrary and solely dependent on whether a PMOS or NMOS is being used as the FET.*

The combination of Applicant's admitted prior art/Chow/Funaba and Emerson are analogous because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Emerson's FET isolation buffers and hot-plug controller within Applicant's admitted prior art/Chow/Funaba's memory module system.

The motivation for doing so would have been to easily and safely remove the failing RAM module from its connector without disturbing normal operation of the computer system (Emerson, col. 10, lines 48-51).

Therefore, it would have been obvious to combine Applicant's admitted prior art, Chow, Funaba, and Emerson for the benefit of obtaining the invention as specified in claim 9.

47. **As per claim 27**, Emerson discloses in replacing an arbitrary memory module, turning ON an FET switch, which is provided in association with said memory module to be replaced, for short-circuiting or opening a bus which is disconnected by removing

said memory module, and turning OFF said FET switch provided in association with the other memory modules (col. 7, lines 12-25; col. 10, lines 37-45; col. 9, lines 38-41; Fig. 4, elements 160 and 164). *Please see the citation notes for claim 9 above.*

48. Claims 10 and 28 are rejected under 35 U.S.C. 103(a) as being obvious over Applicant's admitted prior art in view of Lasker and Funaba as applied to claims 4 and 22 above, and in further view of Emerson.

49. **As per claim 10**, the combination of Applicant's admitted prior art/Lasker/Funaba discloses all the limitations of claim 10 except said short-circuit device is an FET switch, which is provided in association with said memory modules, respectively, for short-circuiting or opening bus connection which is disconnected by removing said memory module,

and in replacing an arbitrary memory module, said control device generates a control signal for turning ON the FET switch provided in association with said memory module to be replaced and turning OFF the FET switches provided in association with the other memory modules.

Emerson discloses said short-circuit device is an FET switch, which is provided in association with said memory modules, respectively, for short-circuiting or opening bus connection which is disconnected by removing said memory module (col. 7, lines 12-25; Fig. 4, element 160), *Please see the citation note for the similar limitation in claim 9 above.*

and in replacing an arbitrary memory module, said control device generates a control signal for turning ON the FET switch provided in association with said memory

module to be replaced and turning OFF the FET switches provided in association with the other memory modules (col. 10, lines 37-45; col. 9, lines 38-41; Fig. 4, elements 160 and 164). *Please see the citation note for the similar limitation in claim 9 above.*

The combination of Applicant's admitted prior art/Lasker/Funaba and Emerson are analogous because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Emerson's FET isolation buffers and hot-plug controller within Applicant's admitted prior art/Lasker/Funaba's memory module system.

The motivation for doing so would have been to easily and safely remove the failing RAM module from its connector without disturbing normal operation of the computer system (Emerson, col. 10, lines 48-51).

Therefore, it would have been obvious to combine Applicant's admitted prior art, Lasker, Funaba, and Emerson for the benefit of obtaining the invention as specified in claim 10.

50. **As per claim 28**, Emerson discloses in replacing an arbitrary memory module, turning ON an FET switch, which is provided in association with said memory module to be replaced, for short-circuiting or opening a bus which is disconnected by removing said memory module, and turning OFF said FET switch provided in association with the other memory modules (col. 7, lines 12-25; col. 10, lines 37-45; col. 9, lines 38-41; Fig. 4, elements 160 and 164). *Please see the citation notes for claim 9 above.*

51. Claims 11 and 29 are rejected under 35 U.S.C. 103(a) as b ing obvious ov r Applicant's admitted prior art in view of Lasker and Funaba as applied to claims 5 and 23 above, and in further view of Emerson.

52. **As per claim 11**, the combination of Applicant's admitted prior art/Lasker/Funaba discloses all the limitations of claim 11 except said short-circuit device is an FET switch, which is provided in association with said memory modules, respectively, for short-circuiting or opening bus connection which is disconnected by removing said memory module,

and in replacing an arbitrary memory module, said control device generates a control signal for turning ON the FET switch provided in association with said memory module to be replaced and turning OFF the FET switches provided in association with the other memory modules.

Emerson discloses said short-circuit device is an FET switch, which is provided in association with said memory modules, respectively, for short-circuiting or opening bus connection which is disconnected by removing said memory module (col. 7, lines 12-25; Fig. 4, element 160), *Please see the citation note for the similar limitation in claim 9 above.*

and in replacing an arbitrary memory module, said control device generates a control signal for turning ON the FET switch provided in association with said memory module to be replaced and turning OFF the FET switches provided in association with the other memory modules (col. 10, lines 37-45; col. 9, lines 38-41; Fig. 4, elements 160 and 164). *Please see the citation note for the similar limitation in claim 9 above.*

Please see the 103 rejection of claim 10 above for the reasons to combine Applicant's admitted prior art, Lasker, Funaba, and Emerson.

53. **As per claim 29**, Emerson discloses in replacing an arbitrary memory module, turning ON an FET switch, which is provided in association with said memory module to be replaced, for short-circuiting or opening a bus which is disconnected by removing said memory module, and turning OFF said FET switch provided in association with the other memory modules (col. 7, lines 12-25; col. 10, lines 37-45; col. 9, lines 38-41; Fig. 4, elements 160 and 164). *Please see the citation notes for claim 9 above.*

54. **Claims 12 and 30 are rejected under 35 U.S.C. 103(a) as being obvious over Applicant's admitted prior art in view of Chow and Funaba as applied to claims 3 and 21 above, and in further view of Greeff et al. (U.S. Patent Application Publication 2002/0083255).**

55. **As per claim 12**, the combination of the combination of Applicant's admitted prior art/Chow/Funaba discloses all the limitations of claim 12 except said short-circuit device is a connector, which is provided in association with said memory modules, respectively, and is provided with short pins which short-circuits bus connection, which is disconnected by removing said memory module, at the time when said memory module is removed, and releases the short-circuit at the time when said memory module is inserted.

Greeff discloses said short-circuit device is a connector, which is provided in association with said memory modules, respectively, and is provided with short pins which short-circuits bus connection, which is disconnected by removing said memory

module, at the time when said memory module is removed, and releases the short-circuit at the time when said memory module is inserted (paragraph 0069, lines 1-4; Fig. 8, element 55). *It should be noted that "continuity module" is analogous to "connector." It should also be noted that at the time a new memory module is inserted it is inherently required the continuity module release the short-circuit.*

The combination of Applicant's admitted prior art/Chow/Funaba and Greeff are analogous because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Greeff's continuity connector within Applicant's admitted prior art/Chow/Funaba's memory module system.

The motivation for doing so would have been to mitigate bus reflections caused by electrical stubs by connecting contemporaneously-selected system components in a stub-less or substantially stubless configuration using switches, thus improving the performance of a memory bus (Greeff, paragraph 0008, lines 1-6).

Therefore, it would have been obvious to combine Applicant's admitted prior art, Chow, Funaba, and Greeff for the benefit of obtaining the invention as specified in claim 12.

56. **As per claim 30**, Greeff discloses in replacing an arbitrary memory module, short-circuiting short pins, which are provided in a connector corresponding to said memory module to be replaced, for short-circuiting or opening a bus which is disconnected by removing said memory module to be replaced, and releasing the short-

circuit of said short pins provided in association with the other memory modules (paragraph 0069, lines 1-4; Fig. 8, element 55). *Please see the citation note for claim 12 above.*

57. **Claims 13 and 31 are rejected under 35 U.S.C. 103(a) as being obvious over Applicant's admitted prior art in view of Lasker and Funaba as applied to claims 4 and 22 above, and in further view of Greeff.**

58. **As per claim 13**, the combination of the combination of Applicant's admitted prior art/Lasker/Funaba discloses all the limitations of claim 12 except said short-circuit device is a connector, which is provided in association with said memory modules, respectively, and is provided with short pins which short-circuits bus connection, which is disconnected by removing said memory module, at the time when said memory module is removed, and releases the short-circuit at the time when said memory module is inserted.

Greeff discloses said short-circuit device is a connector, which is provided in association with said memory modules, respectively, and is provided with short pins which short-circuits bus connection, which is disconnected by removing said memory module, at the time when said memory module is removed, and releases the short-circuit at the time when said memory module is inserted (paragraph 0069, lines 1-4; Fig. 8, element 55). *Please see the citation note for claim 12 above.*

The combination of Applicant's admitted prior art/Lasker/Funaba and Greeff are analogous because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Greeff's continuity connector within Applicant's admitted prior art/Lasker/Funaba's memory module system.

The motivation for doing so would have been to mitigate bus reflections caused by electrical stubs by connecting contemporaneously-selected system components in a stub-less or substantially stubless configuration using switches, thus improving the performance of a memory bus (Greeff, paragraph 0008, lines 1-6).

Therefore, it would have been obvious to combine Applicant's admitted prior art, Lasker, Funaba, and Greeff for the benefit of obtaining the invention as specified in claim 13.

59. **As per claim 31**, Greeff discloses in replacing an arbitrary memory module, short-circuiting short pins, which are provided in a connector corresponding to said memory module to be replaced, for short-circuiting or opening a bus which is disconnected by removing said memory module to be replaced, and releasing the short-circuit of said short pins provided in association with the other memory modules (paragraph 0069, lines 1-4; Fig. 8, element 55). *Please see the citation note for claim 12 above.*

60. **Claims 14 and 32 are rejected under 35 U.S.C. 103(a) as being obvious over Applicant's admitted prior art in view of Lasker and Funaba as applied to claims 5 and 23 above, and in further view of Emerson.**

61. **As per claim 14**, the combination of the combination of Applicant's admitted prior art/Lasker/Funaba discloses all the limitations of claim 12 except said short-circuit

device is a connector, which is provided in association with said memory modules, respectively, and is provided with short pins which short-circuits bus connection, which is disconnected by removing said memory module, at the time when said memory module is removed, and releases the short-circuit at the time when said memory module is inserted.

Greeff discloses said short-circuit device is a connector, which is provided in association with said memory modules, respectively, and is provided with short pins which short-circuits bus connection, which is disconnected by removing said memory module, at the time when said memory module is removed, and releases the short-circuit at the time when said memory module is inserted (paragraph 0069, lines 1-4; Fig. 8, element 55). *Please see the citation note for claim 12 above.*

Please see the 103 rejection of claim 10 above for the reasons to combine Applicant's admitted prior art, Lasker, Funaba, and Greeff.

62. **As per claim 32**, Greeff discloses in replacing an arbitrary memory module, short-circuiting short pins, which are provided in a connector corresponding to said memory module to be replaced, for short-circuiting or opening a bus which is disconnected by removing said memory module to be replaced, and releasing the short-circuit of said short pins provided in association with the other memory modules (paragraph 0069, lines 1-4; Fig. 8, element 55). *Please see the citation note for claim 12 above.*

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1-38** have received a first action on the merits and are subject of a first action non-final.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

1. U.S. Patent 6,263,452 (Jewett et al.) discloses a fault-tolerant computer system with online recovery and reintegration of redundant components.

2. U.S. Patent 6,571,324 (Elkington et al.) discloses a warmswap of failed memory modules and data reconstruction in a mirrored writeback cache system.

3. U.S. Patent 6,766,469 (Larson et al.) discloses a method for replacing a memory module in a segment of a redundant memory system without powering down the memory system.

4. U.S. Patent 6,871,253 (Greeff et al.) discloses a data transmission circuit for a memory subsystem which has a switching circuit that selectively connects or

disconnects two data bus segments to respectively enable data transmission or I/O circuit connection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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